**N** *ational Semiconductor*

# MM54C174/MM74C174 Hex D Flip-Flop

## General Description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to $V_{CC}$ and GND.
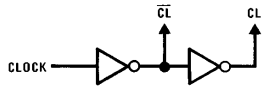
## Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 $V_{CC}$ (typ.)
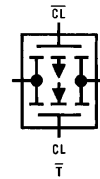- Low power TTL compatibility — Fan out of 2 driving 74L

## Logic and Connection Diagrams
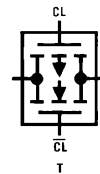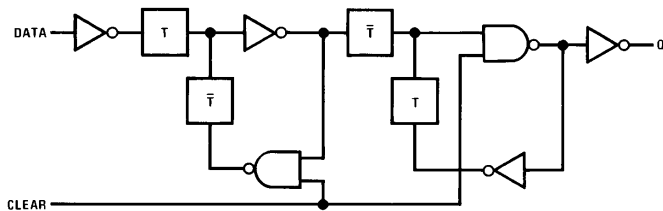


TL/F/5899–2

TL/F/5899–1

TL/F/5899–3

**Dual-In-Line Package**
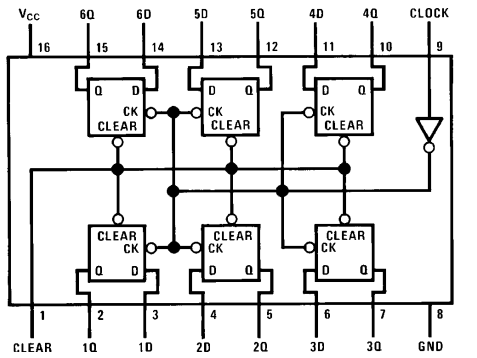


TL/F/5899–4

**Top View**

**Order Number MM54C174 or MM74C174**

## Truth Table

| Inputs | | | Output |
|---|---|---|---|
| Clear | Clock | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $-0.3V$ to $V_{CC} +0.3V$ |

Operating Temperature Range

| | |
|---|---|
| MM54C174 | $-55°C$ to $+125°C$ |
| MM74C174 | $-40°C$ to $+85°C$ |

| | |
|---|---|
| Storage Temperature Range | $-65°C$ to $+150°C$ |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3.0V to 15V |
| Absolute Maximum $V_{CC}$ | 18V |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5V$ | 3.5 | | | V |
| | | $V_{CC} = 10V$ | 8.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5V$ | | | 1.5 | V |
| | | $V_{CC} = 10V$ | | | 2.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5V$, $I_O = -10 \mu A$ | 4.5 | | | V |
| | | $V_{CC} = 10V$, $I_O = -10 \mu A$ | 9.0 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5V$, $I_O = 10 \mu A$ | | | 0.5 | V |
| | | $V_{CC} = 10V$, $I_O = 10 \mu A$ | | | 1.0 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V$, $V_{IN} = 15V$ | | 0.005 | 1.0 | $\mu A$ |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V$, $V_{IN} = 0V$ | $-1.0$ | $-0.005$ | | $\mu A$ |
| $I_{CC}$ | Supply Current | $V_{CC} = 15V$ | | 0.05 | 300 | $\mu A$ |
| **CMOS/LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C, $V_{CC} = 4.5V$ | $V_{CC}-1.5$ | | | V |
| | | 74C, $V_{CC} = 4.75V$ | $V_{CC}-1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C, $V_{CC} = 4.5V$ | | | 0.8 | V |
| | | 74C, $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C, $V_{CC} = 4.5V$, $I_O = -360 \mu A$ | 2.4 | | | V |
| | | 74C, $V_{CC} = 4.75V$, $I_O = -360 \mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C, $V_{CC} = 4.5V$, $I_O = 360 \mu A$ | | | 0.4 | V |
| | | 74C, $V_{CC} = 4.75V$, $I_O = 360 \mu A$ | | | 0.4 | V |
| **OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current (P-Channel) | $V_{CC} = 5V$ $T_A = 25°C$, $V_{OUT} = 0V$ | $-1.75$ | $-3.3$ | | mA |
| $I_{SOURCE}$ | Output Source Current (P-Channel) | $V_{CC} = 10V$ $T_A = 25°C$, $V_{OUT} = 0V$ | $-8.0$ | $-15$ | | mA |
| $I_{SINK}$ | Output Sink Current (N-Channel) | $V_{CC} = 5V$ $T_A = 25°C$, $V_{OUT} = 0V$ | 1.75 | 3.6 | | mA |
| $I_{SINK}$ | Output Sink Current (N-Channel) | $V_{CC} = 5V$ $T_A = 25°C$, $V_{OUT} = 0V$ | 8.0 | 16 | | mA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

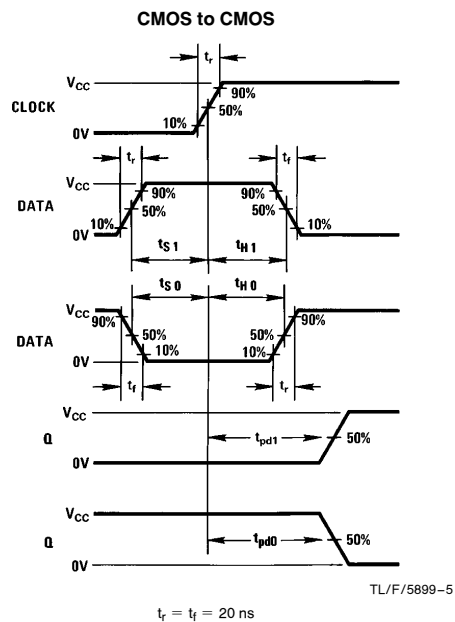| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 150<br>70 | 300<br>110 | ns<br>ns |
| $t_{pd}$ | Propagation Delay Time to a Logical "0" from Clear | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 110<br>50 | 300<br>110 | ns<br>ns |
| $t_{S1}$, $t_{S0}$ | Time Prior to Clock Pulse that Data Must be Present | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 75<br>25 | | | ns<br>ns |
| $t_{H1}$, $t_{H0}$ | Time after Clock Pulse that Data Must be Held | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 0<br>0 | −10<br>−5.0 | | ns<br>ns |
| $t_W$ | Minimum Clock Pulse Width | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 50<br>35 | 250<br>100 | ns<br>ns |
| $t_W$ | Minimum Clear Pulse Width | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 65<br>35 | 140<br>70 | ns<br>ns |
| $t_r$, $t_f$ | Maximum Clock Rise and Fall Time | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 15<br>5.0 | >1200<br>>1200 | | μs<br>μs |
| $f_{MAX}$ | Maximum Clock Frequency | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 2.0<br>5.0 | 6.5<br>12 | | MHz<br>MHz |
| $C_{IN}$ | Input Capacitance | Clear Input (Note 2)<br>Any Other Input | | 11<br>5.0 | | pF<br>pF |
| $C_{PD}$ | Power Dissipation Capacitance | Per Package (Note 3) | | 95 | | pF |

*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
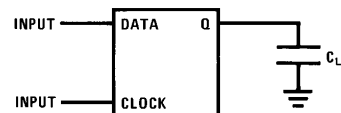
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.
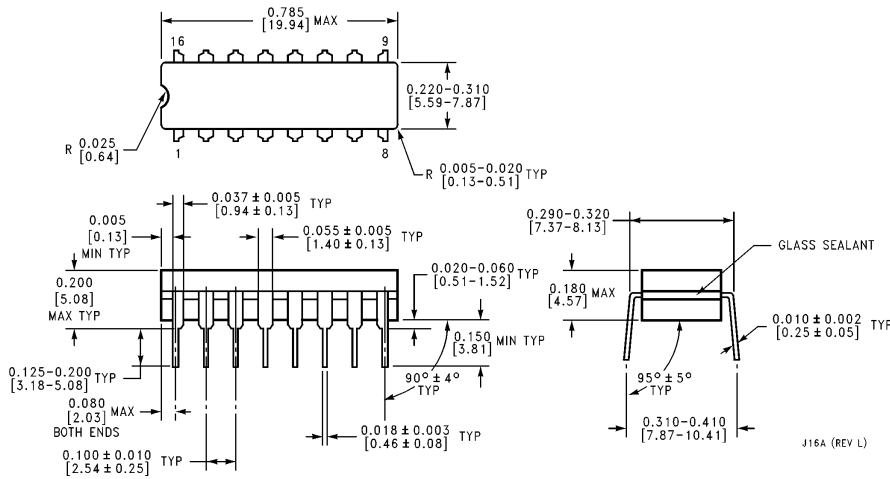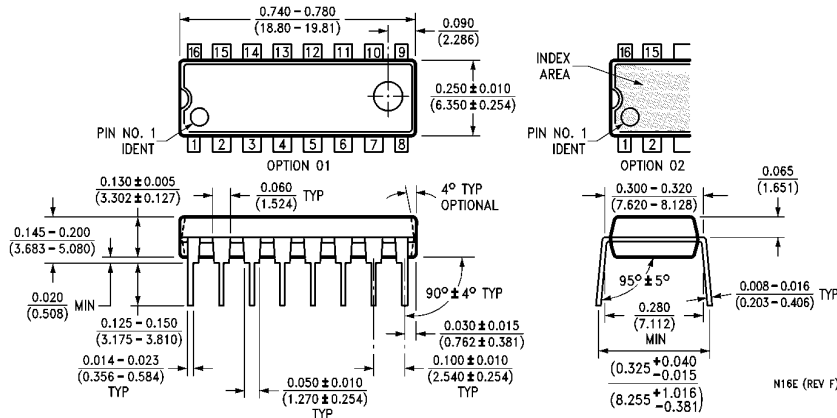
## Switching Time Waveforms

### CMOS to CMOS



TL/F/5899–5

$t_r = t_f = 20$ ns

## AC Test Circuit



TL/F/5899–6

## Physical Dimensions inches (millimeters)

0.785
[19.94] MAX

16          9

0.220–0.310
[5.59–7.87]

R 0.025
[0.64]

1          8

R 0.005–0.020
[0.13–0.51] TYP

0.037 ± 0.005
[0.94 ± 0.13] TYP

0.005
[0.13]
MIN TYP

0.055 ± 0.005
[1.40 ± 0.13] TYP

0.200
[5.08]
MAX TYP

0.020–0.060
[0.51–1.52] TYP

0.290–0.320
[7.37–8.13]

GLASS SEALANT

0.180
[4.57] MAX

0.010 ± 0.002
[0.25 ± 0.05] TYP

0.150
[3.81] MIN TYP

0.125–0.200
[3.18–5.08] TYP

90° ± 4°
TYP

95° ± 5°
TYP

0.080
[2.03] MAX
BOTH ENDS

0.018 ± 0.003
[0.46 ± 0.08] TYP

0.310–0.410
[7.87–10.41]

0.100 ± 0.010
[2.54 ± 0.25] TYP

J16A (REV L)

**Ceramic Dual-In-Line Package (J)**
**Order Number MM54C174J or MM74C174J**
**NS Package Number J16A**

0.740–0.780
(18.80–19.81)

0.090
(2.286)

16 15 14 13 12 11 10 9

0.250 ± 0.010
(6.350 ± 0.254)

INDEX
AREA

16 15

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

PIN NO. 1
IDENT

1 2

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.300–0.320
(7.620–8.128)

0.145–0.200
(3.683–5.080)

95° ± 5°

0.008–0.016
(0.203–0.406) TYP

0.020
(0.508) MIN

90° ± 4° TYP

0.280
(7.112) MIN

0.125–0.150
(3.175–3.810)

0.030 ± 0.015
(0.762 ± 0.381)

$(0.325 {}^{+0.040}_{-0.015})$

0.014–0.023
(0.356–0.584)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

$(8.255 {}^{+1.016}_{-0.381})$

N16E (REV F)

0.050 ± 0.010
(1.270 ± 0.254)
TYP

**Molded Dual-In-Line Package (N)**
**Order Number MM54C174N or MM74C174N**
**NS Package Number N16E**